ECE6332 Project Design Review I

Liang Wang *liang@cs.virginia.edu*

1 Simulation Results

Due to the failure of access to the customized PTM, I can not submit any simulation results for this design review.

2 Report

The progress of the project is quite limited. The group was formed and finalized on this Monday. Moreover, I came up with the problem accessing the customized PTM library files. So I have not run any simulations yet. Since it is close to the next deadline (for proposal), I plan to use standard PTM to go through the whole simulation flow as the first step. After access issue is solved (probably the next week), I could easily switch the design to the customized PTM. Either way, I would manage to got some simulation results for the proposal.

Tasks before the proposal

1. Simulate the ALU of OpenRISC with standard PTM. The object for this simulation is mainly for flow setup.
2. Simulate the ALU of OpenRISC with customized PTM. (Hopefully)

Tasks following the proposal

1. Simulate the ALU of OpenRISC with PTM at 45, 32, and 22nm. Sweep voltage from its nominal value to a little bit below threshold. Investigate maximum frequency, dynamic power and static power.
2. If the ALU is too big for Monte Carlo simulation, figure out a representative paths in ALU, replace ALU with this smaller logic path for the following simulations.
3. Monte Carlo simulation with process variation. Investigate distributions of maximum frequency, dynamic power, and static power.
4. Monte Carlo simulation with threshold voltage variation. Investigate distributions of maximum frequency, dynamic power, and static power.

3 Publications Summary

In [1], Dreslinski et al. presented an extensive overview of near-threshold computing (NTC). The paper demonstrated NTC's benefit of low dynamic power consumption and higher energy efficiency. However, there are a couple of issues associated with NTC. Firstly, the switching speed of a transistor slows down due to small over-drive voltage (supply voltage minus threshold voltage). Secondly, a single transistor is more sensitive to threshold variation when supply voltage is getting close to its threshold, leading to a significant increase in performance variation. Finally, variations in process, temperature and voltage makes the functionality of circuits more vulnerable, especially for SRAM. In addition to pointing out those issues, Dreslinsk et al. had surveyed and summarized various techniques to accommodate those issues. My project is motivated by the second issue of performance variation mentioned in this paper. My project proposes to study the performance variation in future technology nodes with PTM. The proposed project will study the performance impact due to variations of threshold voltage and supplying voltage, considering global process variation and temperature.

[2] presented a testchip with Adaptive Body-bias (ABB) to cope with Die-to-Die and Within-Die variations. The idea of ABB is based on reversed body-bias (RBB) and forward body-bias (FBB), for which RBB changes bias voltage to reduce the leakage power when the circuit is in standby, and FBB increase the performance when the circuit is active. By applying both techniques adaptively, the paper reported a reduction in σ of the die frequency distribution by 7x. Although my proposed project is not targeted at techniques to deal with variations, ABB proposed in this paper helps me understand the problem and extends my knowledge base with an effective approach to deal with performance variation.

[3] proposed a model to describe the maximum clock frequency (FMAX) distribution of a microprocessor. Validation result suggested that within-die variations impact the mean of FMAX and die-to-die variations determine the majority of the FMAX variance. By applying the model to further scaled technology nodes, the paper predicted within-die variations impose significant impact on performance. In the worst case, performance improvement across technology generation would be cancelled by severe within-die variations. This paper reminds me to consider both within-die and die-to-die variations, or core-to-core, within-core, and die-to-die variations for today's multicore architecture.

[4] studied parameter variations and their impacts on circuit design and microarchitecture. The paper investigated three sources of variations, including process variations, supply voltage variations, and temperature variation. Moreover, Borkar et al. showed the impact of those variations to the circuit and microarchitecture, as well as corresponding techniques to tolerate variations. This paper reminds me to include temperature variation in my proposed project.

References

[1] R. G. Dreslinski, M. Wieckowski, D. Blaauw, D. Sylvester, and T. Mudge, "Near-Threshold Computing: Reclaiming Moore's Law Through Energy Efficient Integrated Circuits," *Proceedings of the IEEE, Special Issue on Ultra-Low Power Circuit Technology*, vol. 98, pp. 253–266, February 2010.

[2] J. Tschanz, J. Kao, S. Narendra, R. Nair, D. Antoniadis, A. Chandrakasan, and V. De, "Adaptive Body Bias for Reducing Impacts of Die-to-Die and Within-Die Parameter Variations on Microprocessor Frequency and Leakage," in *IEEE International Solid-State Circuits Conference*, ISSCC '02, 2002.

[3] K. Bowman, S. Duvall, and J. Meindl, "Impact of die-to-die and within-die parameter fluctuations on the maximum clock frequency distribution for gigascale integration," *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 183–190, Feburary 2002.

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